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Mike Wens
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Design and Implementation of Fully-Integrated Inductive DC-DC Converters in Standard CMOS

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ANALOG CIRCUITS AND SIGNAL PROCESSING

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Dr. Mike Wens
ESAT-MICAS
Dept. Elektrotechniek
K.U. Leuven
Room 91.22, Kasteelpark
Arenberg 10
Leuven B-3001
Belgium
Mike.Wens@esat.kuleuven.be

Prof. Dr. Michiel Steyaert
ESAT-MICAS
Dept. Elektrotechniek
K.U. Leuven
Kardinaal Mercierlaan 94
Heverlee B-3001
Belgium
michiel.steyaert@esat.kuleuven.ac.be

Series Editors:
Mohammed Ismail
205 Dreese Laboratory
Department of Electrical Engineering
The Ohio State University
2015 Neil Avenue
Columbus, OH 43210
USA

Mohamad Sawan
Electrical Engineering Department
École Polytechnique de Montréal
Montréal, QC
Canada

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To my wife Larissa and our daughter Anna

Preface

Technological progress in the semiconductor industry has led to a revolution towards new advanced, miniaturized, intelligent, battery-operated and wireless electronic applications. The base of this still ongoing revolution, commonly known as Moore's law, is the ability to manufacture ever decreasing transistor sizes onto a CMOS chip. In other words, the transistor density increases, leading to larger quantity of transistors which can be integrated onto the same single chip die area. As a consequence, more functionality can be integrated onto a single chip die, leading to Systems-on-Chip (SoC) and reducing the total system cost. Indeed, the cost of electronic applications depends in a inverse-proportional fashion on the degree of on-chip integration, which is the main drive for CMOS scaling.

A SoC requires both analog and digital circuitry to be combined in order for it to be able to interact with the analog world. Nevertheless, it is usually processed in a native digital CMOS technology. These CMOS technologies are optimized for the integration of large-scale digital circuits, using very small transistors and low power supply voltages to reduce the power consumption. Beside for the purpose of decreasing the (dynamic) power consumption, the power supply voltage of deep-submicron CMOS technologies is also limited due to the physically very thin gate-oxide of the transistors. This thin gate-oxide, of which the thickness may merely be a few atom layers, would otherwise suffer electrical breakdown. However, the analog circuitry generally needs higher power supply voltages, compared to the digital circuitry. For instance, a power amplifier needs a higher supply voltage to deliver sufficient power into the communication medium. Also, analog signal processing blocks require a higher supply voltage to achieve the desired Signal-to-Noise-Ratio (SNR).

Due to the trend towards electronic applications of portable and wireless nature, (rechargeable) batteries are mandatory to provide the required energy. Although also prone to innovation and improvement, the battery voltage does not scale with the CMOS technology power supply voltages. Obviously, this is due to their physical and chemical constraints. Moreover, their energy density remains limited, limiting the available power and/or the autonomy of the application. Therefore, it is clear that power-management on a SoC-scale is mandatory for ensuring the ongoing feasibility of these applications.

Matching the battery voltage to the required power supply voltage(s) of the SoC can essentially be done in two ways. The first method, which can only be used when the battery voltage is higher than the required power supply voltage(s), is the use of linear voltage converters. This method is very often applied in current state-of-the-art applications, due to the simplicity to integrated it onto the SoC and its low associated cost. However, the excess energy from the battery voltage is dissipated in the form of waste heat, negatively influencing the autonomy and/or physical size of the application. The second method, putting no constraints to the battery voltage, is the use of switched-mode Direct-Current to Direct-Current (DC-DC) voltage converters. These converters are able to increase or decrease the battery voltage in a power-efficient fashion, leading to potentially higher battery autonomies. As a drawback, these switched-mode DC-DC converters are more complex and difficult to integrate onto the SoC, which is why they still require off-chip electronic components, such as inductors and capacitors.

The focus of the presented work is to integrate the switched-mode DC-DC converters onto the SoC, thus reducing both the number of external components and the Printed Circuit Board (PCB) footprint area. However, the poor electrical properties (low Q-factors) of on-chip inductors and capacitors and their low associated values (nH, nF) poses many difficulties, potentially compromising the power conversion efficiency advantage. Combing both the concepts of monolithic SoC integration and achieving a maximal (overall) power conversion efficiency, is the key to success. Moreover, to minimize the costs, the power density of the fully-integrated DC-DC converter is to be maximized.

To achieve these goals a firm theoretical base on the matter of DC-DC conversion is provided, leading to the optimal inductive DC-DC converter topology choices. An extensive mathematical steady-state model is deduced, in order to accurately predict both the trade-offs and performance limits of the inductive DC-DC converters. A further increase the performance of DC-DC converters is achieved through the design of novel control techniques, which are particularly optimized for high-frequency monolithic inductive DC-DC converters. Finally, the theory and simulations are verified and validated through the realization of seven monolithic inductive CMOS DC-DC converters. As such, the highest power density and Efficiency Enhancement Factor (EEF) over a linear voltage converter are obtained, in addition to the feasibility proofing of various novel concepts.

The authors also wish to express their gratitude to all persons who have contributed to this scientific research and the resulting book. We would like to thank Prof. R. Puers and Prof. W. Dehaene for their useful comments. In addition we would like to thank the colleagues of the ESAT-MICAS laboratories of K.U. Leuven for both the direct and indirect contributions to the presented work. Finally, we thank our families for their unconditional support and patience.

Leuven

Mike Wens
Michiel Steyaert

Contents

Abbreviations and Symbols

Abbreviations

AC	Alternating-Current
AC-AC	Alternating-Current to Alternating-Current
AC-DC	Alternating-Current to Direct-Current
ADC	Analog-to-Digital Converter
BCM	Boundary Conduction Mode
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
BJT	Bipolar Junction Transistor
BW	BandWidth
CB	Conduction Boundary
CFL	Compact Fluorescent Lamps
CM	Conduction Mode
CCM	Continuous Conduction Mode
CMOS	Complementary Metal-Oxide Semiconductor
COOT	Constant On/Off-Time
CRT	Cathode Ray Tube
DAC	Digital-to-Analog Converter
DC	Direct-Current
DC-AC	Direct-Current to Alternating-Current
DC-DC	Direct-Current to Direct-Current
DCM	Discontinuous Conduction Mode
DIL	Dual In Line
EEF	Efficiency Enhancement Factor
EMI	Electro Magnetic Interference
FAIMS	High-Field Asymmetric waveform Ion Mobility Spectrometry
FET	Field-Effect Transistor
ESI	Electro-Spray Ionization
ESL	Electric Series inductance
ESR	Electric Series Resistance
FOX	Field Oxide
F^2SCOOT	Feed-Forward Semi-Constant On/Off-Time

GBW	Gain BandWidth
GND	GrouND
HF	High Frequency
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
LDO	Low Drop-Out
LIDAR	Laser Imaging Detection And Ranging
LiION	Lithium-ION
ME1	Metal-1
MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
MOS	Metal-Oxide Semiconductor
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
n-MOSFET	n-channel Metal-Oxide Semiconductor Field-Effect Transistor
MS	Mass Spectrometry
MUX	Multi-PleXer
NPN	n-type p-type n-type transition
OPAMP	OPerational AMPlifier
OTA	Operational Transconductance Amplifier
OX1	Oxide-1
PC	Personal Computer
PCB	Printed Circuit Board
PFC	Power Factor Correction
PFM	Pulse Frequency Modulation
p-MOSFET	p-channel Metal-Oxide Semiconductor Field-Effect Transistor
PNP	p-type n-type p-type transition
PSRR	Power Supply Rejection Ratio
PTC	Positive temperature coefficient
PWM	Pulse Width Modulation
Q.E.D.	Quod Erat Demonstrandum
RC	Resistor-Capacitor
RF	Radio-Frequency
RL	Resistor-Inductor
RLC	Resistor-Inductor-Capacitor
RMS	Root-Mean-Square
SCOOT	Semi-Constant On/Off-Time
SEPIC	Single-Ended Primary-Inductance Converter
SiGe	Silicon-Germanium
SIMO	Single-Inductor Multiple-Output
SMOC	Series Multiple-Output Converter
SMOS	Type of healthy sandwich
SMPS	Switched-Mode Power Supply
SoC	System-on-Chip
SPICE	Simulation Program with Integrated Circuit Emphasis

SRR	Supply Rejection Ratio
SW	Switch

Symbols and Quantities

A	Area
A_C	On-chip capacitor area
A_C^+	Positive charge balance area
A_C^-	Negative charge balance area
A_L	Perpendicular projected area of the inductor windings
A_L^+	Positive volt-second balance area
A_L^-	Negative volt-second balance area
arccos	Arc cosine
$A_\varnothing$	Perpendicular cross-sectional area
$A_{\varnothing\_eff}$	Effective $A_\varnothing$
C	Capacitance
C_{eq}	Equivalent capacitance
cos	Cosine
C_{db}	Parasitic drain-bulk capacitance
C_{dec}	Input decouple capacitance
C_{gb}	Parasitic gate-bulk capacitance
C_{gd}	Parasitic gate-drain capacitance
C_{gc}	Parasitic gate-source capacitance
C_{gg}	Parasitic gate capacitance
C_{g_min}	Parasitic gate of a minimal size inverter
C_{sb}	Parasitic source-bulk capacitance
C_{in}	Input capacitance
C_{out}	Output capacitance
C_{tot}	Total capacitance
C_{out_tot}	Total output capacitance
C_{out_1}	Capacitance of output 1
C_{pad}	Parasitic substrate capacitance of a bonding pad
C_{par}	Parasitic capacitance
C_{sub}	Parasitic substrate winding capacitance
C_1	Capacitance 1
d	Thickness
d	Pitch between two conductors
d_{ox}	Thickness of the oxide
e	Euler's constant: 2.718281828...
E_{C_in}	Energy stored in C
E_{C_out}	Energy delivered by C
$E_C(t)$	Energy stored in C as a function of t
E_{C_1}	Energy stored in C_1
E_{C_2}	Energy stored in C_2
$E_{C_1C_2}$	Energy stored in C_1 and C_2
$E_{C_1 \to C_2}$	Transferred energy from C_1 to C_2
$E_{C_1 \to R}$	Transferred energy from C_1 to R

$E_{C_1 \rightarrow RC}$	Transferred energy from C_1 to RC
EEF	Efficiency Enhancement Factor
$\overline{EEF}$	Mean Efficiency Enhancement Factor
$\widetilde{EEF}$	Weighted Efficiency Enhancement Factor
$EEF(P_{out\_i})$	EEF as a function of the ith P_{out}
E_L	Magnetic energy stored in L
E_{L_in}	Energy stored in L
E_{L_out}	Energy delivered by L
$E_L(t)$	Magnetic energy stored in L as a function of t
$E_L(t)$	Energy stored in L as a function of t
$E_R(t)$	Energy dissipated in R as a function of t
E_{R_2}	Energy dissipated in R_2 in steady-state
$E_{R_2}(t)$	Energy dissipated in R_2 as a function of t
$E_{U_{in}}(t)$	Energy delivered by U_{in} as a function of t
$E_{U_{in} \rightarrow C_1}$	Transferred energy from U_{in} to C_1
$E_{U_{in} \rightarrow C_1 C_2}$	Transferred energy from U_{in} to C_1 and C_2
$E_{U_{in} C_1 \rightarrow C_2}$	Transferred energy from U_{in} and C_1 to C_2
$E_{U_{in} \rightarrow C}(t)$	Transferred energy from U_{in} to C as a function of t
$E_{U_{in} \rightarrow L}(t)$	Transferred energy from U_{in} to L as a function of t
$E_{U_{in} \rightarrow R}(t)$	Transferred energy from U_{in} to R as a function of t
$E_{U_{in} \rightarrow RC}(t)$	Transferred energy from U_{in} to R and C as a function of t
$E_{U_{in} \rightarrow RL}(t)$	Transferred energy from U_{in} to R and L as a function of t
$E_{U_{in} \rightarrow RLC}(t)$	Transferred energy from U_{in} to R, L and C as a function of t
f	Frequency
F	Global effective fan-out
f_{scale}	Scaling factor
f_{SW}	Switching frequency
f_0	Resonance frequency
$g_1\{\}$	Function g_1
$H(f_{SW})$	Transfer function as a function of f_{SW}
I	Current
I_{ak}	Anode-cathode current
I_b	Base current
I_c	Collector current
i_{C_charge}	Charge current through C
$i_{C\_discharge}$	Discharge current through C
I_{C_leak}	Leakage current through C
I_{cs}	Control system supply current
$i_C(t)$	Current through C as a function of t
i_{C1}	Current 1 through C
i_{C2}	Current 2 through C
I_{ds}	Drain-source current
I_e	Emitter current
I_{in}	Input current
I'_{in_max}	Maximum input current

I'_{in_min}	Minimum input current
I_{in_RMS}	RMS input current
$\underline{I_L}$	Mean current through L
I_{L_max}	Maximal current through L
I_{L_min}	Minimal current through L
$i_L(t)$	Current through L as a function of t
$i_L(0)$	Initial current through L
$\underline{I_{out}}$	Output current
$\underline{I_{out}}$	Mean output current
I_{out_RMS}	RMS output current
$I_{out}(t)$	Output current as a function of t
i_{prim}	Current through primary winding
$i_{prim}(s)$	Current through primary winding, in the Laplace-domain
$i_{Rb}(t)$	Current through R_b as a function of t
$i_{Rc}(t)$	Current through R_c as a function of t
i_{sec}	Current through secondary winding
$i_{sec}(s)$	Current through secondary winding, in the Laplace-domain
i_{SW}	Current through SW
$\underline{I_{SW1\_RMS}}$	RMS current through $SW1$
$\underline{i_{SW2}}$	Mean current through $SW2$
$i_{SW2}(t)$	Current through $SW2$ as a function of t
$i(t)$	Current as a function of t
k	Voltage conversion ratio
K	Form-factor fitting parameter
$k(f_{SW})$	Voltage conversion ratio as a function of f_{SW}
k_{lin}	Voltage conversion ratio of a linear voltage converter
k_{lin_max}	Maximal voltage conversion ratio of a linear voltage converter
k_M	Magnetic coupling factor
k_{SW}	Voltage conversion ratio of a switched-mode voltage converter
$k(\delta)$	Voltage conversion ratio as a function of δ
ℓ	Length of a conductor
L	Inductance
L_{Cs}	Parasitic series inductance of C
lim	Limit
L_{line}	Metal line length
L_M	Magnetizing inductance
ln	Natural logarithm
L_n	Gate-length of an nMOSFET
L_{p_buff}	L_p of a buffer
$\ell_{overlap}$	Overlapping length of two conductors
L_p	Gate-length of an pMOSFET
L_{prim}	Primary winding inductance
L_{sec}	Secondary winding inductance
L_{self}	Self inductance
L_{tot}	Total inductance

L_{track}	Length of a metal track
L_1	Inductance 1
$\mathfrak{L}^{-1}$	Inverse Laplace-transform
M	Mutual inductance
M^+	Positive mutual inductance
M^-	Negative mutual inductance
n	Number of stages/phases
N_a	Doping concentration
n_{prim}	Number of turns in the primary winding
n_{sec}	Number of turns in the secondary winding
n_{Tr}	Winding turn ratio
n_1	Number of turns of winding 1
P_{buff_cpar}	Power loss in parasitic capacitances in buffers
P_{buff_short}	Power loss due to short-circuit current in buffers
P_C	Power for charging a capacitor
P_{Df}	Diode forward conduction power loss
P_{diss}	Dissipated power
P_{in}	Input power
P_{in_lin}	Input power of a linear DC-DC voltage converter
P_{in_SW}	Input power of switched-mode DC-DC voltage converter
P_{L_Csub}	Parasitic substrate capacitance power loss of an inductor
P_{out}	Output power
P'_{out}	Real output power
P_{out_lin}	Output power of a linear DC-DC voltage converter
P_{out_max}	Maximal output power
P_{out_SW}	Output power of a switched-mode DC-DC voltage converter
P_{Rcs}	Parasitic series resistance power loss
P_{Rcp}	Parasitic parallel resistance power loss
P_{Rin}	Power loss in R_{in}
P_{Ron}	Power loss in R_{on}
P_{Rout}	Power loss in R_{out}
P_{Rsw1}	Power loss in R_{SW1}
P_{tf_SW1}	Fall-time power loss of $SW1$
P_{tr_SW1}	Rise-time power loss of $SW1$
Q	Q-factor
Q_d	Charge in the drain
Q_g	Charge in the gate
Q_s	Charge in the source
Q_{in}	Stored charge
Q_{out}	Delivered charge
r	Perpendicular cross-section radius a round conductor
R	Resistance
R_a	Equivalent resistance
R_b	Equivalent resistance
$R_{bondwire}$	Parasitic series resistance of a bondwire

R_c	Equivalent resistance
$R_{channel\square}$	Square-resistance of the induced channel
R_{Cdec}	Parasitic series resistance of C_{dec}
R_{cont_f}	Parasitic series resistance of gate contacts
R_{cont_ds}	Parasitic series resistance of drain/source contacts
R_{Cp}	Parasitic parallel resistance of C
R_{Cs}	Parasitic series resistance of C
R_e	Equivalent load resistance
R_{eq}	Equivalent resistance
R_{in}	Input resistance
R_{in}	Parasitic series resistance of U_{in}
R_L	Load resistance
R'_L	Real load resistance
R_{left}	Conductor series resistance, seen from the left
R_{Ls}	Parasitic series resistance of L
$R_{Ls@T}$	R_{Ls} at temperature T
$R_{Ls@T+\Delta T}$	R_{Ls} at temperature $T + \Delta T$
R_{line}	Line resistance
R_{loss}	Additional loss resistance
$R_{n+\square}$	Square-resistance of n^+-region
R_{on}	On-resistance
$R_{on@T}$	R_{on} at temperature T
$R_{on@T+\Delta T}$	R_{on} at temperature $T + \Delta T$
R_{on_n}	On-resistance of an n-MOSFET
R_{on_p}	On-resistance of an p-MOSFET
R_{out}	Parasitic output resistance
$R_{ploy\square}$	Square-resistance of poly-silicon
R_{right}	Conductor series resistance, seen from the right
R_{sen}	Sense resistance
R_{series}	Variable series resistance of a series voltage converter
R_{shunt}	Variable shunt resistance of a shunt voltage converter
R_{SW1}	Parasitic series resistance of SW_1
R_{track}	Parasitic series resistance of a metal track
R_{via}	Parasitic via series resistance
R_{via_tot}	Total parasitic via series resistance
R_0	Output resistance at f_0
$R_\square$	Square-resistance
s	Laplace-transform operator
sin	Sine
t	Time
T	Period
T	Temperature
$t_{a\rightarrow b}$	Time from point a to point b
$t_{a\rightarrow c}$	Time from point a to point c
$t_{b\rightarrow c}$	Time from point b to point c

t_d	Dead-time
t_f	Fall-time
t_{f_SW1}	Fall-time SW_1
t_{flank}	Mean rise/fall-time
t_{on}	On-time
t_{off}	Off-time
t_{off_real}	Real off-time
t_{ox}	MOSFET gate-oxide thickness
t_r	Rise-time
$t_{r/f}$	Rise/fall-time
t_{r_SW1}	Rise-time SW_1
Tr	Transformer
t_{SW}	Switching/Charging time
t_{zero1}	Intersect time 1 with the X-axis
t_1	Time 1
U	Voltage
U_{be}	Base-emitter voltage
U_{ce}	Collector-emitter voltage
U_{C_max}	Maximal voltage over C
U_{C_min}	Minimal voltage over C
$u_C(t)$	Voltage over C as a function of t
$U_C(T)$	Voltage over C at the end of T
$U_C(0)$	Initial voltage over C
U_{dd}	Nominal technology supply voltage
U_{Df}	Diode forward voltage drop
U_{ds}	Drain-source voltage
U_{dsatp}	Drain-source saturation voltage of a p-MOSFET
U_{dsn}	Drain-source voltage of an n-MOSFET
U_{err}	Error-voltage
U_{gb}	Gate-bulk voltage
U_{g_od}	Gate-overdrive voltage
U_{gs}	Gate-source voltage
U_{gsn}	Gate-source voltage of an n-MOSFET
U_{in}	Input voltage
U'_{in_max}	Maximum input voltage
U'_{in_min}	Minimum input voltage
U_{in_peak}	Peak value of U_{in}
$u_L(t)$	Voltage over L as a function of t
U_{L1}	Voltage 1 over L
U_{offset}	Offset voltage
$\underline{U_{out}}$	Output voltage
$\overline{U_{out}}$	Mean output voltage
U_{out_max}	Maximal output voltage
U_{out_min}	Minimal output voltage
U_{out_RMS}	RMS output voltage

U'_{out_RMS}	Real RMS output voltage
$u_{out}(t)$	Output voltage as a function of t
$u_{out}(x)$	Output voltage as a function of x
$\hat{u}_{out}(x)$	Output voltage amplitude as a function of x
$\hat{u}_{out}(\theta)$	Output voltage amplitude as a function of θ
U_{prim}	Voltage over the primary winding
U_{out_ptp}	Peak-to-peak output voltage
$u_{Ra}(t)$	Voltage over R_a as a function of t
$u_{Rb}(t)$	Voltage over R_b as a function of t
$u_{Rc}(t)$	Voltage over R_c as a function of t
$u_{RCp}(t)$	Voltage over R_{Cp} as a function of t
$u_{RCs}(t)$	Voltage over R_{Cs} as a function of t
U_{ref}	Reference voltage
$u_R(t)$	Voltage over R as a function of t
U_{sb}	Source-bulk voltage
U_{sen}	Sense voltage
U_{sec}	Voltage over the secondary winding
u_{SW}	Voltage over SW
U_{SW_3}	Voltage over SW_3
U_{tria}	Triangular waveform voltage
V_t	Threshold voltage
W_{drain}	Drain-width
W_n	Gate-width of an nMOSFET
W_p	Gate-width of an pMOSFET
W_{p_buff}	W_p of a buffer
W_{source}	Source-width
W_{track}	Width of a metal track
x	ΔU_{out} approximation variable
Z_{in}	Input impedance
Z_k	Impedance ratio
Z_{out}	Output impedance
Z_1	Impedance 1
α	Resistance temperature coefficient
$\alpha(P_{out})$	Power activity probability distribution
δ	Duty-cycle
δ_{skin}	Skin-depth
ΔI_{in}	Input current ripple
ΔI_L	Current ripple through L
ΔI_{L_tot}	Total current ripple through L
ΔI_{L_1}	Current ripple through L_1
ΔP_{in}	Input power difference
ΔT	Temperature difference
ΔU	Voltage difference
ΔU_C	Voltage swing over a capacitor
ΔU_{in}	Input voltage ripple

ΔU_L	Voltage swing over an inductor
ΔU_{out}	Output voltage ripple
$\Delta U_{out}(\delta)$	Output voltage ripple as a function of δ
ΔQ	Charge difference
ΔQ_{SW}	Transferred charge in one switch cycle
$\Delta\eta$	Power conversion efficiency difference
ϵ	Dielectric permittivity
ϵ_0	Permittivity of vacuum
ϵ_{r_ox}	Relative permittivity of an oxide
η	Power conversion efficiency
η_{C_charge}	Energy charging efficiency of C
$\eta_{C\_charge}(t)$	η_{C_charge} as a function of t
η_{L_charge}	Energy charging efficiency of L
$\eta_{L\_charge}(t)$	η_{L_charge} as a function of t
$\eta_{RLC\_charge}(t)$	η_{C_charge} in an RLC-circuit as a function of t
η_{lin}	Power conversion efficiency of a linear DC-DC voltage converter
η_{sp_down}	Power conversion efficiency of a step-down charge-pump
η_{sp_up}	Power conversion efficiency of a step-up charge-pump
η_{SW}	Power conversion efficiency of a switched-mode DC-DC converter
η_{SW_max}	Maximal η_{SW}
η_{Tr}	Power conversion efficiency of an ideal transformer
$\eta_{Tr}(t)$	η_{Tr} as a function of t
η_{Φ_1}	Energy conversion efficiency of Φ_1
γ	Thermal resistance
Φ_1	Phase 1
κ	CMOS technology scaling factor
λ_p	Early voltage of a p-MOSFET
μ_n	n-carrier mobility
μ_p	p-carrier mobility
μ	Magnetic Permeability
μ_r	Relative permeability
π	Circumference/diameter ratio of a circle: 3.141592654...
ρ	Resistivity
τ_C	Time constant of an RC-circuit
τ_L	Time constant of an RL-circuit
τ_{LC}	Time constant of an RLC-circuit
τ_{Tr}	Time constant of the primary winding of a transformer
θ	Phase difference
ω_{LC}	Angular frequency of an RLC-circuit
Υ	ΔU_{out} approximation function
#*fingers*	Number of gate fingers of a MOS capacitor
$\#C_{out\_1}$	Total required C to implement C_{out_1}
$\#C_{out\_tot}$	Total required C to implement C_{out_tot}
#*seg*	Number of segments
#*via*	Number of vias

∞	Infinite
■	Q.E.D.
✔	A benefit
✘	A drawback

List of Figures