

ACSP · Analog Circuits And Signal Processing

Mike Wens  
Michiel Steyaert

Design and Implementation  
of Fully-Integrated  
Inductive DC-DC Converters  
in Standard CMOS

 Springer

# Design and Implementation of Fully-Integrated Inductive DC-DC Converters in Standard CMOS

# **ANALOG CIRCUITS AND SIGNAL PROCESSING**

*Series Editors:*

**Mohammed Ismail.** *The Ohio State University*

**Mohamad Sawan.** *École Polytechnique de Montréal*

For other titles published in this series, go to  
[www.springer.com/series/7381](http://www.springer.com/series/7381)

Mike Wens • Michiel Steyaert

# Design and Implementation of Fully-Integrated Inductive DC-DC Converters in Standard CMOS

 Springer

Dr. Mike Wens  
ESAT-MICAS  
Dept. Elektrotechniek  
K.U. Leuven  
Room 91.22, Kasteelpark  
Arenberg 10  
Leuven B-3001  
Belgium  
[Mike.Wens@esat.kuleuven.be](mailto:Mike.Wens@esat.kuleuven.be)

Prof. Dr. Michiel Steyaert  
ESAT-MICAS  
Dept. Elektrotechniek  
K.U. Leuven  
Kardinaal Mercierlaan 94  
Heverlee B-3001  
Belgium  
[michiel.steyaert@esat.kuleuven.ac.be](mailto:michiel.steyaert@esat.kuleuven.ac.be)

*Series Editors:*

Mohammed Ismail  
205 Dreese Laboratory  
Department of Electrical Engineering  
The Ohio State University  
2015 Neil Avenue  
Columbus, OH 43210  
USA

Mohamad Sawan  
Electrical Engineering Department  
École Polytechnique de Montréal  
Montréal, QC  
Canada

ISBN 978-94-007-1435-9  
DOI 10.1007/978-94-007-1436-6  
Springer Dordrecht Heidelberg London New York

e-ISBN 978-94-007-1436-6

Library of Congress Control Number: 2011928697

© Springer Science+Business Media B.V. 2011

No part of this work may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electronic, mechanical, photocopying, microfilming, recording or otherwise, without written permission from the Publisher, with the exception of any material supplied specifically for the purpose of being entered and executed on a computer system, for exclusive use by the purchaser of the work.

*Cover design:* VTeX UAB, Lithuania

Printed on acid-free paper

Springer is part of Springer Science+Business Media ([www.springer.com](http://www.springer.com))

*To my wife Larissa and our daughter Anna*

# Preface

Technological progress in the semiconductor industry has led to a revolution towards new advanced, miniaturized, intelligent, battery-operated and wireless electronic applications. The base of this still ongoing revolution, commonly known as Moore's law, is the ability to manufacture ever decreasing transistor sizes onto a CMOS chip. In other words, the transistor density increases, leading to larger quantity of transistors which can be integrated onto the same single chip die area. As a consequence, more functionality can be integrated onto a single chip die, leading to Systems-on-Chip (SoC) and reducing the total system cost. Indeed, the cost of electronic applications depends in an inverse-proportional fashion on the degree of on-chip integration, which is the main drive for CMOS scaling.

A SoC requires both analog and digital circuitry to be combined in order for it to be able to interact with the analog world. Nevertheless, it is usually processed in a native digital CMOS technology. These CMOS technologies are optimized for the integration of large-scale digital circuits, using very small transistors and low power supply voltages to reduce the power consumption. Beside for the purpose of decreasing the (dynamic) power consumption, the power supply voltage of deep-submicron CMOS technologies is also limited due to the physically very thin gate-oxide of the transistors. This thin gate-oxide, of which the thickness may merely be a few atom layers, would otherwise suffer electrical breakdown. However, the analog circuitry generally needs higher power supply voltages, compared to the digital circuitry. For instance, a power amplifier needs a higher supply voltage to deliver sufficient power into the communication medium. Also, analog signal processing blocks require a higher supply voltage to achieve the desired Signal-to-Noise-Ratio (SNR).

Due to the trend towards electronic applications of portable and wireless nature, (rechargeable) batteries are mandatory to provide the required energy. Although also prone to innovation and improvement, the battery voltage does not scale with the CMOS technology power supply voltages. Obviously, this is due to their physical and chemical constraints. Moreover, their energy density remains limited, limiting the available power and/or the autonomy of the application. Therefore, it is clear that power-management on a SoC-scale is mandatory for ensuring the ongoing feasibility of these applications.

Matching the battery voltage to the required power supply voltage(s) of the SoC can essentially be done in two ways. The first method, which can only be used when the battery voltage is higher than the required power supply voltage(s), is the use of linear voltage converters. This method is very often applied in current state-of-the-art applications, due to the simplicity to integrate it onto the SoC and its low associated cost. However, the excess energy from the battery voltage is dissipated in the form of waste heat, negatively influencing the autonomy and/or physical size of the application. The second method, putting no constraints to the battery voltage, is the use of switched-mode Direct-Current to Direct-Current (DC-DC) voltage converters. These converters are able to increase or decrease the battery voltage in a power-efficient fashion, leading to potentially higher battery autonomies. As a drawback, these switched-mode DC-DC converters are more complex and difficult to integrate onto the SoC, which is why they still require off-chip electronic components, such as inductors and capacitors.

The focus of the presented work is to integrate the switched-mode DC-DC converters onto the SoC, thus reducing both the number of external components and the Printed Circuit Board (PCB) footprint area. However, the poor electrical properties (low Q-factors) of on-chip inductors and capacitors and their low associated values (nH, nF) poses many difficulties, potentially compromising the power conversion efficiency advantage. Combining both the concepts of monolithic SoC integration and achieving a maximal (overall) power conversion efficiency, is the key to success. Moreover, to minimize the costs, the power density of the fully-integrated DC-DC converter is to be maximized.

To achieve these goals a firm theoretical base on the matter of DC-DC conversion is provided, leading to the optimal inductive DC-DC converter topology choices. An extensive mathematical steady-state model is deduced, in order to accurately predict both the trade-offs and performance limits of the inductive DC-DC converters. A further increase the performance of DC-DC converters is achieved through the design of novel control techniques, which are particularly optimized for high-frequency monolithic inductive DC-DC converters. Finally, the theory and simulations are verified and validated through the realization of seven monolithic inductive CMOS DC-DC converters. As such, the highest power density and Efficiency Enhancement Factor (EEF) over a linear voltage converter are obtained, in addition to the feasibility proofing of various novel concepts.

The authors also wish to express their gratitude to all persons who have contributed to this scientific research and the resulting book. We would like to thank Prof. R. Puers and Prof. W. Dehaene for their useful comments. In addition we would like to thank the colleagues of the ESAT-MICAS laboratories of K.U. Leuven for both the direct and indirect contributions to the presented work. Finally, we thank our families for their unconditional support and patience.

Leuven

Mike Wens  
Michiel Steyaert



# Contents

<b>1</b>	<b>Introduction</b>	1
1.1	The Origin of DC-DC Converters	2
1.1.1	Basic Considerations	2
1.1.2	Historical Notes	3
1.2	Low Power DC-DC Converter Applications	9
1.2.1	Mains-Operated	10
1.2.2	Battery-Operated	11
1.3	Monolithic DC-DC Converters: A Glimpse into the Future	14
1.3.1	CMOS Technology	15
1.3.2	The Challenges	20
1.4	Structural Outline	23
1.5	Conclusions	24
<b>2</b>	<b>Basic DC-DC Converter Theory</b>	27
2.1	Linear Voltage Converters	27
2.1.1	Series Converter	28
2.1.2	Shunt Converter	29
2.2	Charge-Pump DC-DC Converters	31
2.2.1	On Capacitors	32
2.2.2	Series-Parallel Step-Down Converter	34
2.2.3	Series-Parallel Step-Up Converter	38
2.3	Inductive Type DC-DC Converters	41
2.3.1	On Inductors	41
2.3.2	Inductors and Capacitors: The Combination	44
2.3.3	Reflections on Steady-State Calculation Methods	49
2.4	INTERMEZZO: The Efficiency Enhancement Factor	59
2.4.1	The Concept	59
2.4.2	Interpretations	61
2.5	Conclusions	62
<b>3</b>	<b>Inductive DC-DC Converter Topologies</b>	65
3.1	Step-Down Converters	65

3.1.1	Buck Converter . . . . .	66
3.1.2	Bridge Converter . . . . .	72
3.1.3	Three-Level Buck Converter . . . . .	74
3.1.4	Buck <sup>2</sup> Converter . . . . .	77
3.1.5	Watkins-Johnson Converter . . . . .	79
3.1.6	Step-Down Converter Summary . . . . .	81
3.2	Step-Up Converters . . . . .	82
3.2.1	Boost Converter . . . . .	84
3.2.2	Current-Fed Bridge Converter . . . . .	85
3.2.3	Inverse Watkins-Johnson Converter . . . . .	86
3.2.4	Step-Up Converter Summary . . . . .	88
3.3	Step-Up/Down Converters . . . . .	90
3.3.1	Buck-Boost Converter . . . . .	91
3.3.2	Non-inverting Buck-Boost Converter . . . . .	92
3.3.3	Ćuk Converter . . . . .	93
3.3.4	SEPIC Converter . . . . .	94
3.3.5	Zeta Converter . . . . .	95
3.3.6	Step-Up/Down Converter Summary . . . . .	97
3.4	Other Types of Inductive DC-DC Converters . . . . .	99
3.4.1	Galvanic Separated Converters . . . . .	99
3.4.2	Resonant DC-DC Converters . . . . .	104
3.5	Topology Variations . . . . .	107
3.5.1	Multi-phase DC-DC Converters . . . . .	107
3.5.2	Single-Inductor Multiple-Output DC-DC Converters . . . . .	115
3.5.3	On-Chip Topologies . . . . .	118
3.6	Conclusions . . . . .	121
<b>4</b>	<b>A Mathematical Model: Boost and Buck Converter . . . . .</b>	<b>123</b>
4.1	Second-Order Model: Boost and Buck Converter . . . . .	124
4.1.1	Differential Equations: Boost Converter . . . . .	124
4.1.2	Calculating the Output Voltage: Boost Converter . . . . .	126
4.1.3	Differential Equations: Buck Converter . . . . .	131
4.1.4	Calculating the Output Voltage: Buck Converter . . . . .	132
4.2	Non-ideal Converter Components Models . . . . .	135
4.2.1	Inductor . . . . .	136
4.2.2	Capacitor . . . . .	142
4.2.3	Switches . . . . .	146
4.2.4	Buffers . . . . .	152
4.2.5	Interconnect . . . . .	154
4.3	Temperature Effects . . . . .	158
4.3.1	Inductor . . . . .	159
4.3.2	Switches . . . . .	159
4.4	The Final Model Flow . . . . .	160
4.4.1	Inserting the Dynamic Losses . . . . .	161
4.4.2	Inserting the Temperature Effects . . . . .	163
4.4.3	Reflections on Design . . . . .	164
4.5	Conclusions . . . . .	167

- 5 Control Systems . . . . . 169**
  - 5.1 Inductive Type Converter Control Strategies . . . . . 170
    - 5.1.1 Pulse Width Modulation . . . . . 170
    - 5.1.2 Pulse Frequency Modulation . . . . . 175
    - 5.1.3 Pulse Width Modulation vs. Pulse Frequency Modulation . 176
  - 5.2 Constant On/Off-Time: COOT . . . . . 181
    - 5.2.1 The COOT Concept . . . . . 181
    - 5.2.2 Single-Phase, Single-Output Implementations . . . . . 184
    - 5.2.3 Single-Phase, Two-Output SIMO Implementation . . . . . 188
  - 5.3 Semi-Constant On/Off-Time: SCOOT . . . . . 193
    - 5.3.1 The SCOOT Concept . . . . . 193
    - 5.3.2 Multi-phase Implementations . . . . . 195
  - 5.4 Feed-Forward Semi-Constant On/Off-Time: F<sup>2</sup>-SCOOT . . . . . 203
    - 5.4.1 The F<sup>2</sup>-SCOOT Concept . . . . . 203
    - 5.4.2 Single-Phase, Two-Output Implementation . . . . . 205
  - 5.5 Start-up . . . . . 209
    - 5.5.1 The Concept . . . . . 210
    - 5.5.2 Implementations . . . . . 210
  - 5.6 Conclusions . . . . . 211
- 6 Implementations . . . . . 213**
  - 6.1 Monolithic Converter Components . . . . . 214
    - 6.1.1 Inductor . . . . . 214
    - 6.1.2 Capacitor . . . . . 216
    - 6.1.3 Switches . . . . . 220
  - 6.2 On Measuring DC-DC Converters . . . . . 224
    - 6.2.1 Main Principles . . . . . 224
    - 6.2.2 Practical Example . . . . . 226
  - 6.3 Boost Converters . . . . . 228
    - 6.3.1 Bondwire, Single-Phase, Single-Output . . . . . 228
    - 6.3.2 Metal-Track, Single-Phase, Two-Output SIMO . . . . . 232
  - 6.4 Buck Converters . . . . . 235
    - 6.4.1 Bondwire, Single-Phase, Single-Output . . . . . 236
    - 6.4.2 Metal-Track, Single-Phase, Single-Output . . . . . 240
    - 6.4.3 Metal-Track, Four-Phase, Single Output . . . . . 244
    - 6.4.4 Metal-Track, Four-Phase, Two-Output SMOC . . . . . 248
    - 6.4.5 Bondwire, Single-Phase, Two-Output SMOC . . . . . 250
  - 6.5 Comparison to Other Work . . . . . 254
    - 6.5.1 Inductive Step-Up Converters . . . . . 255
    - 6.5.2 Inductive Step-Down Converters . . . . . 256
  - 6.6 Conclusions . . . . . 259
- 7 General Conclusions . . . . . 261**
  - 7.1 Conclusions . . . . . 261
  - 7.2 Remaining Challenges . . . . . 263

**References** . . . . . 265

**Index** . . . . . 273

# Abbreviations and Symbols

## *Abbreviations*

AC	Alternating-Current
AC-AC	Alternating-Current to Alternating-Current
AC-DC	Alternating-Current to Direct-Current
ADC	Analog-to-Digital Converter
BCM	Boundary Conduction Mode
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
BJT	Bipolar Junction Transistor
BW	BandWidth
CB	Conduction Boundary
CFL	Compact Fluorescent Lamps
CM	Conduction Mode
CCM	Continuous Conduction Mode
CMOS	Complementary Metal-Oxide Semiconductor
COOT	Constant On/Off-Time
CRT	Cathode Ray Tube
DAC	Digital-to-Analog Converter
DC	Direct-Current
DC-AC	Direct-Current to Alternating-Current
DC-DC	Direct-Current to Direct-Current
DCM	Discontinuous Conduction Mode
DIL	Dual In Line
EEF	Efficiency Enhancement Factor
EMI	Electro Magnetic Interference
FAIMS	High-Field Asymmetric waveform Ion Mobility Spectrometry
FET	Field-Effect Transistor
ESI	Electro-Spray Ionization
ESL	Electric Series inductance
ESR	Electric Series Resistance
FOX	Field Oxide
F <sup>2</sup> SCOOT	Feed-Forward Semi-Constant On/Off-Time

GBW	Gain BandWidth
GND	GrouND
HF	High Frequency
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
LDO	Low Drop-Out
LIDAR	Laser Imaging Detection And Ranging
LiION	Lithium-ION
ME1	Metal-1
MIM	Metal-Insulator-Metal
MOM	Metal-Oxide-Metal
MOS	Metal-Oxide Semiconductor
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
n-MOSFET	n-channel Metal-Oxide Semiconductor Field-Effect Transistor
MS	Mass Spectrometry
MUX	Multi-PleXer
NPN	<i>n</i> -type <i>p</i> -type <i>n</i> -type transition
OPAMP	OPerational AMPLifier
OTA	Operational Transconductance Amplifier
OX1	Oxide-1
PC	Personal Computer
PCB	Printed Circuit Board
PFC	Power Factor Correction
PFM	Pulse Frequency Modulation
p-MOSFET	p-channel Metal-Oxide Semiconductor Field-Effect Transistor
PNP	<i>p</i> -type <i>n</i> -type <i>p</i> -type transition
PSRR	Power Supply Rejection Ratio
PTC	Positive temperature coefficient
PWM	Pulse Width Modulation
Q.E.D.	Quod Erat Demonstrandum
RC	Resistor-Capacitor
RF	Radio-Frequency
RL	Resistor-Inductor
RLC	Resistor-Inductor-Capacitor
RMS	Root-Mean-Square
SCOOT	Semi-Constant On/Off-Time
SEPIC	Single-Ended Primary-Inductance Converter
SiGe	Silicon-Germanium
SIMO	Single-Inductor Multiple-Output
SMOC	Series Multiple-Output Converter
SMOS	Type of healthy sandwich
SMPS	Switched-Mode Power Supply
SoC	System-on-Chip
SPICE	Simulation Program with Integrated Circuit Emphasis

SRR	Supply Rejection Ratio
SW	Switch

*Symbols and Quantities*

$A$	Area
$A_C$	On-chip capacitor area
$A_C^+$	Positive charge balance area
$A_C^-$	Negative charge balance area
$A_L$	Perpendicular projected area of the inductor windings
$A_L^+$	Positive volt-second balance area
$A_L^-$	Negative volt-second balance area
arccos	Arc cosine
$A_\varnothing$	Perpendicular cross-sectional area
$A_{\varnothing\_eff}$	Effective $A_\varnothing$
$C$	Capacitance
$C_{eq}$	Equivalent capacitance
cos	Cosine
$C_{db}$	Parasitic drain-bulk capacitance
$C_{dec}$	Input decouple capacitance
$C_{gb}$	Parasitic gate-bulk capacitance
$C_{gd}$	Parasitic gate-drain capacitance
$C_{gc}$	Parasitic gate-source capacitance
$C_{gg}$	Parasitic gate capacitance
$C_{g\_min}$	Parasitic gate of a minimal size inverter
$C_{sb}$	Parasitic source-bulk capacitance
$C_{in}$	Input capacitance
$C_{out}$	Output capacitance
$C_{tot}$	Total capacitance
$C_{out\_tot}$	Total output capacitance
$C_{out\_1}$	Capacitance of output 1
$C_{pad}$	Parasitic substrate capacitance of a bonding pad
$C_{par}$	Parasitic capacitance
$C_{sub}$	Parasitic substrate winding capacitance
$C_1$	Capacitance 1
$d$	Thickness
$d$	Pitch between two conductors
$d_{ox}$	Thickness of the oxide
$e$	Euler's constant: 2.718281828...
$E_{C\_in}$	Energy stored in $C$
$E_{C\_out}$	Energy delivered by $C$
$E_C(t)$	Energy stored in $C$ as a function of $t$
$E_{C_1}$	Energy stored in $C_1$
$E_{C_2}$	Energy stored in $C_2$
$E_{C_1C_2}$	Energy stored in $C_1$ and $C_2$
$E_{C_1 \rightarrow C_2}$	Transferred energy from $C_1$ to $C_2$
$E_{C_1 \rightarrow R}$	Transferred energy from $C_1$ to $R$

$E_{C_1 \rightarrow RC}$	Transferred energy from $C_1$ to $RC$
$EEF$	Efficiency Enhancement Factor
$\overline{EEF}$	Mean Efficiency Enhancement Factor
$\widetilde{EEF}$	Weighted Efficiency Enhancement Factor
$EEF(P_{out\_i})$	$EEF$ as a function of the $i$ th $P_{out}$
$E_L$	Magnetic energy stored in $L$
$E_{L\_in}$	Energy stored in $L$
$E_{L\_out}$	Energy delivered by $L$
$E_L(t)$	Magnetic energy stored in $L$ as a function of $t$
$E_L(t)$	Energy stored in $L$ as a function of $t$
$E_R(t)$	Energy dissipated in $R$ as a function of $t$
$E_{R_2}$	Energy dissipated in $R_2$ in steady-state
$E_{R_2}(t)$	Energy dissipated in $R_2$ as a function of $t$
$E_{U_{in}}(t)$	Energy delivered by $U_{in}$ as a function of $t$
$E_{U_{in} \rightarrow C_1}$	Transferred energy from $U_{in}$ to $C_1$
$E_{U_{in} \rightarrow C_1 C_2}$	Transferred energy from $U_{in}$ to $C_1$ and $C_2$
$E_{U_{in} C_1 \rightarrow C_2}$	Transferred energy from $U_{in}$ and $C_1$ to $C_2$
$E_{U_{in} \rightarrow C}(t)$	Transferred energy from $U_{in}$ to $C$ as a function of $t$
$E_{U_{in} \rightarrow L}(t)$	Transferred energy from $U_{in}$ to $L$ as a function of $t$
$E_{U_{in} \rightarrow R}(t)$	Transferred energy from $U_{in}$ to $R$ as a function of $t$
$E_{U_{in} \rightarrow RC}(t)$	Transferred energy from $U_{in}$ to $R$ and $C$ as a function of $t$
$E_{U_{in} \rightarrow RL}(t)$	Transferred energy from $U_{in}$ to $R$ and $L$ as a function of $t$
$E_{U_{in} \rightarrow RLC}(t)$	Transferred energy from $U_{in}$ to $R$ , $L$ and $C$ as a function of $t$
$f$	Frequency
$F$	Global effective fan-out
$f_{scale}$	Scaling factor
$f_{SW}$	Switching frequency
$f_0$	Resonance frequency
$g_1\{\}$	Function $g_1$
$H(f_{SW})$	Transfer function as a function of $f_{SW}$
$I$	Current
$I_{ak}$	Anode-cathode current
$I_b$	Base current
$I_c$	Collector current
$i_{C\_charge}$	Charge current through $C$
$i_{C\_discharge}$	Discharge current through $C$
$I_{C\_leak}$	Leakage current through $C$
$I_{cs}$	Control system supply current
$i_C(t)$	Current through $C$ as a function of $t$
$i_{C1}$	Current 1 through $C$
$i_{C2}$	Current 2 through $C$
$I_{ds}$	Drain-source current
$I_e$	Emitter current
$I_{in}$	Input current
$I'_{in\_max}$	Maximum input current



$I'_{in\_min}$	Minimum input current
$I_{in\_RMS}$	RMS input current
$I_L$	Mean current through $L$
$I_{L\_max}$	Maximal current through $L$
$I_{L\_min}$	Minimal current through $L$
$i_L(t)$	Current through $L$ as a function of $t$
$i_L(0)$	Initial current through $L$
$I_{out}$	Output current
$I_{out}$	Mean output current
$I_{out\_RMS}$	RMS output current
$I_{out}(t)$	Output current as a function of $t$
$i_{prim}$	Current through primary winding
$i_{prim}(s)$	Current through primary winding, in the Laplace-domain
$i_{Rb}(t)$	Current through $R_b$ as a function of $t$
$i_{Rc}(t)$	Current through $R_c$ as a function of $t$
$i_{sec}$	Current through secondary winding
$i_{sec}(s)$	Current through secondary winding, in the Laplace-domain
$i_{SW}$	Current through $SW$
$I_{SW1\_RMS}$	RMS current through $SW1$
$i_{SW2}$	Mean current through $SW2$
$i_{SW2}(t)$	Current through $SW2$ as a function of $t$
$i(t)$	Current as a function of $t$
$k$	Voltage conversion ratio
$K$	Form-factor fitting parameter
$k(f_{SW})$	Voltage conversion ratio as a function of $f_{SW}$
$k_{lin}$	Voltage conversion ratio of a linear voltage converter
$k_{lin\_max}$	Maximal voltage conversion ratio of a linear voltage converter
$k_M$	Magnetic coupling factor
$k_{SW}$	Voltage conversion ratio of a switched-mode voltage converter
$k(\delta)$	Voltage conversion ratio as a function of $\delta$
$\ell$	Length of a conductor
$L$	Inductance
$L_{Cs}$	Parasitic series inductance of $C$
lim	Limit
$L_{line}$	Metal line length
$L_M$	Magnetizing inductance
ln	Natural logarithm
$L_n$	Gate-length of an nMOSFET
$L_{p\_buff}$	$L_p$ of a buffer
$\ell_{overlap}$	Overlapping length of two conductors
$L_p$	Gate-length of an pMOSFET
$L_{prim}$	Primary winding inductance
$L_{sec}$	Secondary winding inductance
$L_{self}$	Self inductance
$L_{tot}$	Total inductance

$L_{track}$	Length of a metal track
$L_1$	Inductance 1
$\mathcal{L}^{-1}$	Inverse Laplace-transform
$M$	Mutual inductance
$M^+$	Positive mutual inductance
$M^-$	Negative mutual inductance
$n$	Number of stages/phases
$N_a$	Doping concentration
$n_{prim}$	Number of turns in the primary winding
$n_{sec}$	Number of turns in the secondary winding
$n_{Tr}$	Winding turn ratio
$n_1$	Number of turns of winding 1
$P_{buff\_cpar}$	Power loss in parasitic capacitances in buffers
$P_{buff\_short}$	Power loss due to short-circuit current in buffers
$P_C$	Power for charging a capacitor
$P_{Df}$	Diode forward conduction power loss
$P_{diss}$	Dissipated power
$P_{in}$	Input power
$P_{in\_lin}$	Input power of a linear DC-DC voltage converter
$P_{in\_SW}$	Input power of switched-mode DC-DC voltage converter
$P_{L\_Csub}$	Parasitic substrate capacitance power loss of an inductor
$P_{out}$	Output power
$P'_{out}$	Real output power
$P_{out\_lin}$	Output power of a linear DC-DC voltage converter
$P_{out\_max}$	Maximal output power
$P_{out\_SW}$	Output power of a switched-mode DC-DC voltage converter
$P_{Rcs}$	Parasitic series resistance power loss
$P_{Rcp}$	Parasitic parallel resistance power loss
$P_{Rin}$	Power loss in $R_{in}$
$P_{Ron}$	Power loss in $R_{on}$
$P_{Rout}$	Power loss in $R_{out}$
$P_{Rsw1}$	Power loss in $R_{sw1}$
$P_{tf\_SW1}$	Fall-time power loss of SW1
$P_{tr\_SW1}$	Rise-time power loss of SW1
$Q$	Q-factor
$Q_d$	Charge in the drain
$Q_g$	Charge in the gate
$Q_s$	Charge in the source
$Q_{in}$	Stored charge
$Q_{out}$	Delivered charge
$r$	Perpendicular cross-section radius a round conductor
$R$	Resistance
$R_a$	Equivalent resistance
$R_b$	Equivalent resistance
$R_{bondwire}$	Parasitic series resistance of a bondwire

$R_c$	Equivalent resistance
$R_{channel\Box}$	Square-resistance of the induced channel
$R_{Cdec}$	Parasitic series resistance of $C_{dec}$
$R_{cont\_f}$	Parasitic series resistance of gate contacts
$R_{cont\_ds}$	Parasitic series resistance of drain/source contacts
$R_{Cp}$	Parasitic parallel resistance of $C$
$R_{Cs}$	Parasitic series resistance of $C$
$R_e$	Equivalent load resistance
$R_{eq}$	Equivalent resistance
$R_{in}$	Input resistance
$R_{in}$	Parasitic series resistance of $U_{in}$
$R_L$	Load resistance
$R'_L$	Real load resistance
$R_{left}$	Conductor series resistance, seen from the left
$R_{Ls}$	Parasitic series resistance of $L$
$R_{Ls@T}$	$R_{Ls}$ at temperature $T$
$R_{Ls@T+\Delta T}$	$R_{Ls}$ at temperature $T + \Delta T$
$R_{line}$	Line resistance
$R_{loss}$	Additional loss resistance
$R_{n+\Box}$	Square-resistance of $n^+$ -region
$R_{on}$	On-resistance
$R_{on@T}$	$R_{on}$ at temperature $T$
$R_{on@T+\Delta T}$	$R_{on}$ at temperature $T + \Delta T$
$R_{on\_n}$	On-resistance of an n-MOSFET
$R_{on\_p}$	On-resistance of an p-MOSFET
$R_{out}$	Parasitic output resistance
$R_{poly\Box}$	Square-resistance of poly-silicon
$R_{right}$	Conductor series resistance, seen from the right
$R_{sen}$	Sense resistance
$R_{series}$	Variable series resistance of a series voltage converter
$R_{shunt}$	Variable shunt resistance of a shunt voltage converter
$R_{SW1}$	Parasitic series resistance of $SW_1$
$R_{track}$	Parasitic series resistance of a metal track
$R_{via}$	Parasitic via series resistance
$R_{via\_tot}$	Total parasitic via series resistance
$R_0$	Output resistance at $f_0$
$R\Box$	Square-resistance
$s$	Laplace-transform operator
$\sin$	Sine
$t$	Time
$T$	Period
$T$	Temperature
$t_{a\rightarrow b}$	Time from point $a$ to point $b$
$t_{a\rightarrow c}$	Time from point $a$ to point $c$
$t_{b\rightarrow c}$	Time from point $b$ to point $c$

$t_d$	Dead-time
$t_f$	Fall-time
$t_{f\_SW1}$	Fall-time $SW_1$
$t_{flank}$	Mean rise/fall-time
$t_{on}$	On-time
$t_{off}$	Off-time
$t_{off\_real}$	Real off-time
$t_{ox}$	MOSFET gate-oxide thickness
$t_r$	Rise-time
$t_{r/f}$	Rise/fall-time
$t_{r\_SW1}$	Rise-time $SW_1$
$Tr$	Transformer
$t_{SW}$	Switching/Charging time
$t_{zerol}$	Intersect time 1 with the X-axis
$t_1$	Time 1
$U$	Voltage
$U_{be}$	Base-emitter voltage
$U_{ce}$	Collector-emitter voltage
$U_{C\_max}$	Maximal voltage over $C$
$U_{C\_min}$	Minimal voltage over $C$
$u_C(t)$	Voltage over $C$ as a function of $t$
$U_C(T)$	Voltage over $C$ at the end of $T$
$U_C(0)$	Initial voltage over $C$
$U_{dd}$	Nominal technology supply voltage
$U_{Df}$	Diode forward voltage drop
$U_{ds}$	Drain-source voltage
$U_{dsatp}$	Drain-source saturation voltage of a p-MOSFET
$U_{dsn}$	Drain-source voltage of an n-MOSFET
$U_{err}$	Error-voltage
$U_{gb}$	Gate-bulk voltage
$U_{g\_od}$	Gate-overdrive voltage
$U_{gs}$	Gate-source voltage
$U_{gsn}$	Gate-source voltage of an n-MOSFET
$U_{in}$	Input voltage
$U'_{in\_max}$	Maximum input voltage
$U'_{in\_min}$	Minimum input voltage
$U_{in\_peak}$	Peak value of $U_{in}$
$u_L(t)$	Voltage over $L$ as a function of $t$
$U_{L1}$	Voltage 1 over $L$
$U_{offset}$	Offset voltage
$U_{out}$	Output voltage
$\overline{U_{out}}$	Mean output voltage
$U_{out\_max}$	Maximal output voltage
$U_{out\_min}$	Minimal output voltage
$U_{out\_RMS}$	RMS output voltage

$U'_{out\_RMS}$	Real RMS output voltage
$u_{out}(t)$	Output voltage as a function of $t$
$u_{out}(x)$	Output voltage as a function of $x$
$\hat{u}_{out}(x)$	Output voltage amplitude as a function of $x$
$\hat{u}_{out}(\theta)$	Output voltage amplitude as a function of $\theta$
$U_{prim}$	Voltage over the primary winding
$U_{out\_ptp}$	Peak-to-peak output voltage
$u_{Ra}(t)$	Voltage over $R_a$ as a function of $t$
$u_{Rb}(t)$	Voltage over $R_b$ as a function of $t$
$u_{Rc}(t)$	Voltage over $R_c$ as a function of $t$
$u_{RCp}(t)$	Voltage over $R_{Cp}$ as a function of $t$
$u_{RCs}(t)$	Voltage over $R_{Cs}$ as a function of $t$
$U_{ref}$	Reference voltage
$u_R(t)$	Voltage over $R$ as a function of $t$
$U_{sb}$	Source-bulk voltage
$U_{sen}$	Sense voltage
$U_{sec}$	Voltage over the secondary winding
$u_{SW}$	Voltage over $SW$
$U_{SW_3}$	Voltage over $SW_3$
$U_{tria}$	Triangular waveform voltage
$V_t$	Threshold voltage
$W_{drain}$	Drain-width
$W_n$	Gate-width of an nMOSFET
$W_p$	Gate-width of an pMOSFET
$W_{p\_buff}$	$W_p$ of a buffer
$W_{source}$	Source-width
$W_{track}$	Width of a metal track
$x$	$\Delta U_{out}$ approximation variable
$Z_{in}$	Input impedance
$Z_k$	Impedance ratio
$Z_{out}$	Output impedance
$Z_1$	Impedance 1
$\alpha$	Resistance temperature coefficient
$\alpha(P_{out})$	Power activity probability distribution
$\delta$	Duty-cycle
$\delta_{skin}$	Skin-depth
$\Delta I_{in}$	Input current ripple
$\Delta I_L$	Current ripple through $L$
$\Delta I_{L\_tot}$	Total current ripple through $L$
$\Delta I_{L\_1}$	Current ripple through $L_1$
$\Delta P_{in}$	Input power difference
$\Delta T$	Temperature difference
$\Delta U$	Voltage difference
$\Delta U_C$	Voltage swing over a capacitor
$\Delta U_{in}$	Input voltage ripple

$\Delta U_L$	Voltage swing over an inductor
$\Delta U_{out}$	Output voltage ripple
$\Delta U_{out}(\delta)$	Output voltage ripple as a function of $\delta$
$\Delta Q$	Charge difference
$\Delta Q_{SW}$	Transferred charge in one switch cycle
$\Delta \eta$	Power conversion efficiency difference
$\epsilon$	Dielectric permittivity
$\epsilon_0$	Permittivity of vacuum
$\epsilon_{r\_ox}$	Relative permittivity of an oxide
$\eta$	Power conversion efficiency
$\eta_{C\_charge}$	Energy charging efficiency of $C$
$\eta_{C\_charge}(t)$	$\eta_{C\_charge}$ as a function of $t$
$\eta_{L\_charge}$	Energy charging efficiency of $L$
$\eta_{L\_charge}(t)$	$\eta_{L\_charge}$ as a function of $t$
$\eta_{RLC\_charge}(t)$	$\eta_{C\_charge}$ in an $RLC$ -circuit as a function of $t$
$\eta_{lin}$	Power conversion efficiency of a linear DC-DC voltage converter
$\eta_{sp\_down}$	Power conversion efficiency of a step-down charge-pump
$\eta_{sp\_up}$	Power conversion efficiency of a step-up charge-pump
$\eta_{SW}$	Power conversion efficiency of a switched-mode DC-DC converter
$\eta_{SW\_max}$	Maximal $\eta_{SW}$
$\eta_{Tr}$	Power conversion efficiency of an ideal transformer
$\eta_{Tr}(t)$	$\eta_{Tr}$ as a function of $t$
$\eta_{\Phi_1}$	Energy conversion efficiency of $\Phi_1$
$\gamma$	Thermal resistance
$\Phi_1$	Phase 1
$\kappa$	CMOS technology scaling factor
$\lambda_p$	Early voltage of a p-MOSFET
$\mu_n$	n-carrier mobility
$\mu_p$	p-carrier mobility
$\mu$	Magnetic Permeability
$\mu_r$	Relative permeability
$\pi$	Circumference/diameter ratio of a circle: 3.141592654...
$\rho$	Resistivity
$\tau_C$	Time constant of an $RC$ -circuit
$\tau_L$	Time constant of an $RL$ -circuit
$\tau_{LC}$	Time constant of an $RLC$ -circuit
$\tau_{Tr}$	Time constant of the primary winding of a transformer
$\theta$	Phase difference
$\omega_{LC}$	Angular frequency of an $RLC$ -circuit
$\Upsilon$	$\Delta U_{out}$ approximation function
$\#fingers$	Number of gate fingers of a MOS capacitor
$\#C_{out\_1}$	Total required $C$ to implement $C_{out\_1}$
$\#C_{out\_tot}$	Total required $C$ to implement $C_{out\_tot}$
$\#seg$	Number of segments
$\#via$	Number of vias

$\infty$	Infinite
■	Q.E.D.
✓	A benefit
✗	A drawback

# List of Figures

Fig. 1.1	A black-box representation of a DC-DC converter . . . . .	2
Fig. 1.2	The power-balance of a DC-DC converter . . . . .	2
Fig. 1.3	The principle of ideal switching . . . . .	3
Fig. 1.4	<b>(a)</b> Faraday’s original 1831 <i>induction ring</i> [ <a href="#">Ins10</a> ] and <b>(b)</b> the schematic representation of the induction ring experiment . . . . .	4
Fig. 1.5	A mechanical rotary DC-AC step-up converter, for powering gas-discharge lamps [ <a href="#">Ran34</a> ] . . . . .	4
Fig. 1.6	<b>(a)</b> A Cockcroft-Walton voltage multiplier build in the year 1937, which was used for an early particle accelerator [ <a href="#">Wik10</a> ]. <b>(b)</b> A half-wave, two-stage Cockcroft-Walton voltage multiplier . . . . .	5
Fig. 1.7	A mechanical vibratory DC-DC step-up converter [ <a href="#">Sta34</a> ] . . . . .	6
Fig. 1.8	A DC-DC step-up converter, using an inverted vacuum-tube triode as primary switch and secondary rectifier [ <a href="#">Haz40</a> ] . . . . .	6
Fig. 1.9	<b>(a)</b> The first commercial vacuum-tube triode: <i>the audion</i> . <b>(b)</b> The schematic symbol of a direct-heated triode and its simplified construction principle . . . . .	7
Fig. 1.10	A transistorized DC-DC step-up converter, for powering a vacuum-tube pentode audio amplifier for a hearing aid device [ <a href="#">Phi53</a> ] . . . . .	8
Fig. 1.11	A two-phase DC-DC step-up converter [ <a href="#">Wes67</a> ] . . . . .	8
Fig. 1.12	<b>(a)</b> The first contact bipolar junction transistor [ <a href="#">Rio10b</a> ] and <b>(b)</b> a schematic cross section of an NPN BJT . . . . .	9
Fig. 1.13	The block-diagram representation of a mains-operated application, using step-down AC-DC converter . . . . .	10
Fig. 1.14	<b>(a)</b> The block diagram of a battery-operated application using a DC-DC step-down converter with external components. <b>(b)</b> The same system implemented as a SoC, with a monolithic DC-DC converter . . . . .	12
Fig. 1.15	<b>(a)</b> The block diagram of a battery-operated application using a DC-DC step-up converter with external components. <b>(b)</b> The same system implemented as a SoC, with a monolithic DC-DC converter . . . . .	14



Fig. 1.16	(a) The first integrated circuit [Lee10b] and (b) the schematic circuit representation [Lee10c] . . . . .	15
Fig. 1.17	(a) The schematic symbol of an n-MOSFET and (b) its schematic perspective cross-section view . . . . .	16
Fig. 1.18	The qualitative behavior for an n-MOSFET of $I_{ds}$ as a function of $U_{ds}$ , for different $U_{gs}$ . . . . .	17
Fig. 1.19	An n-MOSFET ( <i>left</i> ) and a p-MOSFET ( <i>right</i> ) in a six-mask CMOS process. The <i>upper</i> drawings show the lay-out view and the <i>lower</i> ones a cross-section of the according physical devices . . . . .	18
Fig. 1.20	The minimum feature size and the transistor count per chip as a function of time, for Intel CMOS technologies [Boh09] . . . . .	19
Fig. 1.21	A cross-sectional view of the interconnect of the 32 nm Intel CMOS process [Boh10] . . . . .	20
Fig. 1.22	A perspective microphotograph of a DC-DC step-up converter, using a bondwire inductor [Wen07] . . . . .	22
Fig. 1.23	The graphical representation of the structural outline of the dissertation . . . . .	24
Fig. 2.1	(a) The principle of a linear series voltage converter and (b) a simple practical implementation . . . . .	28
Fig. 2.2	(a) The power conversion efficiency $\eta_{lin}$ as a function of the output power $P_{out}$ for a linear series voltage converter, at a constant voltage conversion ratio $k_{lin}$ . The <i>black curve</i> is valid for a zero control system supply current $I_{cs}$ and the <i>gray curve</i> is valid for a non-zero $I_{cs}$ . (b) The power conversion efficiency $\eta_{lin}$ as a function of the voltage conversion ratio $k_{lin}$ for a linear series voltage converter, at a constant output power $P_{out}$ . The <i>black curve</i> is valid for a zero control system supply current $I_{cs}$ and the <i>gray curve</i> is valid for a non-zero $I_{cs}$ . . . . .	29
Fig. 2.3	(a) The principle of a linear shunt voltage converter and (b) a simple practical implementation . . . . .	30
Fig. 2.4	(a) The power conversion efficiency $\eta_{lin}$ as a function of the output power $P_{out}$ for a linear shunt voltage converter, at a constant voltage conversion ratio $k_{lin}$ . The <i>black curve</i> is valid for a zero control system supply current $I_{cs}$ and the <i>gray curve</i> is valid for a non-zero $I_{cs}$ . (b) The power conversion efficiency $\eta_{lin}$ as a function of the voltage conversion ratio $k_{lin}$ for a linear shunt voltage converter, for a constant value of $P_{out} = P_{out\_max}$ . The <i>black curve</i> is valid for a zero control system supply current $I_{cs}$ and the <i>gray curve</i> is valid for a non-zero $I_{cs}$ . . . . .	31
Fig. 2.5	(a) The circuit for charging a capacitor $C$ with a series resistor $R$ by means of a voltage source $U_{in}$ . (b) The voltage $u_C(t)$ over $C$ and the current $i_C(t)$ through $C$ , as a function of time. (c) The energy $E_{U_{in} \rightarrow RC}(t)$ delivered by $U_{in}$ , the energy $E_{U_{in} \rightarrow C}(t)$ stored in $C$ and the energy $E_{U_{in} \rightarrow R}(t)$ dissipated in $R$ , as a function of time . . . . .	32

Fig. 2.6 The energy charging efficiency  $\eta_{C\_charge}$  of a capacitor charged by means of a voltage source  $U_{in}$  as a function of the initial voltage  $U_C(0)$  over the capacitor, for three different charge times  $t$  . . . . . 33

Fig. 2.7 **(a)** The circuit for charging  $C_b$  with  $C_a$ . **(b)** The  $E_{C_a \rightarrow RC_b}$ ,  $E_{C_a \rightarrow C_b}$  and  $E_{C_a \rightarrow R}$  as a function of  $\Delta U = U_{C_a}(0) - U_{C_b}(0)$ , for  $C_a \gg C_b$  and **(c)** for  $C_b \gg C_a$  . . . . . 35

Fig. 2.8 **(a)** The circuit of an ideal series-parallel charge-pump step-down DC-DC converter, together with **(b)** its equivalent charge circuit and **(c)** its equivalent discharge circuit . . . . . 36

Fig. 2.9 The *black curves* show the power conversion efficiency  $\eta_{sp\_down}$  of an ideal series-parallel charge-pump step-down DC-DC converter, as a function of the voltage conversion ratio  $k_{SW}$ , for three different cases of the values of  $C_1$  and  $C_2$ . The *gray curve* shows the power conversion efficiency of a linear series converter, as a function of  $k_{SW}$  . . . . . 38

Fig. 2.10 **(a)** The circuit of an ideal series-parallel charge-pump step-up DC-DC converter, together with **(b)** its equivalent charge circuit and **(c)** its equivalent discharge circuit . . . . . 39

Fig. 2.11 The *black curves* show the power conversion efficiency  $\eta_{sp\_up}$  of an ideal series-parallel charge-pump step-up DC-DC converter, as a function of the voltage conversion ratio  $k_{SW}$ , for three different cases of the values of  $C_1$  and  $C_2$ . The *gray curve* shows the power conversion efficiency  $\eta_{lin}$  of a linear series converter, as a function of  $k_{SW}$  . . . . . 40

Fig. 2.12 **(a)** The circuit for charging an inductor  $L$  in series with a resistor  $R$  by means of a voltage source  $U_{in}$ . **(b)** The voltage  $u_L(t)$  over and the current  $i_L(t)$  through  $L$ , as a function of time. **(c)** The energy  $E_{U_{in} \rightarrow RL}(t)$  delivered by  $U_{in}$ , the energy  $E_{U_{in} \rightarrow L}(t)$  stored in  $L$  and the energy  $E_{U_{in} \rightarrow R}(t)$  dissipated in  $R$ , as a function of time . . . . . 42

Fig. 2.13 The energy charging efficiency  $\eta_{L\_charge}$  of an inductor with a series resistance charged by a voltage source  $U_{in}$ , as a function of the initial current  $I_C(0)$  through the inductor, for three different charge time  $t$  . . . . . 43

Fig. 2.14 The circuit for charging a series inductor  $L$  and a series capacitor  $C$  with a series resistor  $R$ , by means of a voltage source  $U_{in}$  . . . . . 44

Fig. 2.15 **(a)** The current  $i(t)$ , the voltage  $u_L(t)$  over  $L$ , the voltage  $u_R(t)$  over  $R$  and the voltage  $u_C(t)$  over  $C$  as a function of time, for in ideal ( $R = 0$ ) and **(b)** a non-ideal ( $R \neq 0$ ) series  $RLC$ -circuit . . . . . 46

Fig. 2.16 **(a)** The energy  $E_{U_{in} \rightarrow RLC}(t)$  delivered by  $U_{in}$  the energy  $E_L(t)$  stored in  $L$ , the energy  $E_R(t)$  dissipated in  $R$  and the energy  $E_C(t)$  stored in  $C$  as a function of time, for an ideal ( $R = 0$ ) and **(b)** a non-ideal ( $R \neq 0$ ) series  $RLC$ -circuit . . . . . 47

Fig. 2.17 (a) The energy charging efficiency  $\eta_{RLC\_charge}(t)$  of a capacitor in a periodically-damped series  $RLC$ -circuit as a function of time, for different values of the initial voltages  $U_C(0)$  over  $C$  and (b) for different initial currents  $I_L(0)$  through  $L$  . . . . . 48

Fig. 2.18 (a) The circuit of an ideal boost DC-DC converter. (b) The equivalent circuit of the inductor charge phase and (c) the inductor discharge phase . . . . . 50

Fig. 2.19 (a) The convention of the voltage over and the current through a capacitor  $C$  and an inductor  $L$ . (b) The current  $i_C(t)$  through  $C$  and (c) the voltage  $u_L(t)$  over  $L$ , both in energetic equilibrium . . . . . 51

Fig. 2.20 The linearized current  $i_L(t)$  through  $L$ , the linearized voltage  $u_L(t)$  over  $L$ , the linearized current  $i_C(t)$  through  $C$  and the linearized output voltage  $u_{out}(t)$  as a function of time, for an ideal boost converter in CCM . . . . . 52

Fig. 2.21 The voltage conversion ratio  $k(\delta)$  as a function of the duty-cycle  $\delta$ , for an ideal boost converter in CCM . . . . . 53

Fig. 2.22 The linearized current  $i_L(t)$  through  $L$ , the linearized voltage  $u_L(t)$  over  $L$ , the linearized current  $i_C(t)$  through  $C$  and the linearized output voltage  $u_{out}(t)$  as a function of time, for an ideal boost converter in DCM . . . . . 54

Fig. 2.23 The *upper graph* shows the voltage conversion ratio  $k(\delta)$  as a function of the duty-cycle  $\delta$ , where the *black curve* is valid for CCM and the *gray curves* for DCM. In the *lower graph* the *black curve* shows the boundary between the two CMs and the *gray curves* illustrate three numerical examples. These graphs are valid for an ideal DC-DC boost converter . . . . . 58

Fig. 2.24 The *upper graph* shows the power conversion efficiencies  $\eta_{SW}$  and  $\eta_{lin}$  of a switched-mode DC-DC converter and a linear series voltage converter having the same voltage conversion ratio  $k_{lin} = k_{SW}$ , as a function of the output power  $P_{out}$ . The *lower graph* shows the corresponding  $EEF$  and  $\overline{EEF}$ , as a function of  $P_{out}$  . . . . . 61

Fig. 3.1 (a) The circuit of an ideal buck DC-DC converter. (b) The equivalent circuit of the inductor charge phase and (c) the inductor discharge phase . . . . . 67

Fig. 3.2 The linearized  $i_L(t)$ , the linearized  $u_L(t)$ , the linearized  $i_C(t)$  and the linearized  $u_{out}(t)$  as a function of time, for an ideal buck DC-DC converter in CCM . . . . . 68

Fig. 3.3 The linearized  $i_L(t)$ , the linearized  $u_L(t)$ , the linearized  $i_C(t)$  and the linearized  $u_{out}(t)$  as a function of time, for an ideal buck DC-DC converter in DCM . . . . . 69

Fig. 3.4 The *upper graph* shows  $k(\delta)$  as a function of  $\delta$ , where the *black curve* is valid for CCM and the *gray curves* for DCM. In the *lower graph* the *black curve* shows the boundary between the two CMs and the *gray curves* illustrate three numerical examples. These graphs are valid for an ideal DC-DC buck converter . . . . . 70

Fig. 3.5 The circuit of an ideal bridge DC-DC converter . . . . . 73

Fig. 3.6 The voltage conversion ratio  $k(\delta)$  as a function of the duty-cycle  $\delta$ , for a bridge converter in CCM . . . . . 73

Fig. 3.7 The circuit of an ideal three-level buck DC-DC converter . . . . . 75

Fig. 3.8 **(a)** The timing of the four switches of an ideal three-level buck DC-DC converter in CCM, for  $\delta < 0.5$  and **(b)** for  $\delta > 0.5$  . . . . . 75

Fig. 3.9 The circuit of an ideal buck<sup>2</sup> DC-DC converter . . . . . 77

Fig. 3.10 The voltage conversion ratio  $k(\delta)$  as a function of the duty-cycle  $\delta$ , for an ideal buck<sup>2</sup> converter in CCM . . . . . 78

Fig. 3.11 **(a)** The circuit of an ideal Watkins-Johnson DC-DC converter, using an inductor and **(b)** using two coupled inductors . . . . . 80

Fig. 3.12 The voltage conversion ratio  $k(\delta)$  as a function of the duty-cycle  $\delta$ , for a Watkins-Johnson converter in CCM . . . . . 80

Fig. 3.13 The total required capacitance  $C_{tot}$  of five step-down DC-DC converter topologies as a function of the output power  $P_{out}$ . These values are obtained by means of SPICE-simulations, such that the five converters meet with the specifications of Table 3.1 . . . . . 83

Fig. 3.14 The circuit of an ideal current-fed bridge DC-DC converter . . . . . 85

Fig. 3.15 The voltage conversion ratio  $k(\delta)$  as a function of the duty-cycle  $\delta$ , for a current-fed bridge converter in CCM . . . . . 85

Fig. 3.16 **(a)** The circuit of an ideal inverse Watkins-Johnson DC-DC converter, using an inductor and **(b)** using two coupled inductors . . . . . 87

Fig. 3.17 The voltage conversion ratio  $k(\delta)$  as a function of the duty-cycle  $\delta$ , for an inverse Watkins-Johnson converter in CCM . . . . . 87

Fig. 3.18 The total required capacitance  $C_{tot}$  of three DC-DC step-up converter topologies as a function of the output power  $P_{out}$ . These values are obtained by means of SPICE-simulations, such that the three converters meet with the specifications of Table 3.8 . . . . . 90

Fig. 3.19 The circuit of an ideal buck-boost DC-DC converter . . . . . 91

Fig. 3.20 The voltage conversion ratio  $k(\delta)$  as a function of the duty-cycle  $\delta$ , for an ideal buck-boost converter in CCM . . . . . 92

Fig. 3.21 The circuit of an ideal non-inverting buck-boost DC-DC converter . . . . . 92

Fig. 3.22 The voltage conversion ratio  $k(\delta)$  as a function of the duty-cycle  $\delta$ , for an ideal non-inverting buck-boost converter in CCM . . . . . 92

Fig. 3.23 The circuit of an ideal Ćuk DC-DC converter . . . . . 93

Fig. 3.24 The circuit of an ideal SEPIC DC-DC converter . . . . . 94

Fig. 3.25 The circuit of an ideal zeta DC-DC converter . . . . . 96

Fig. 3.26	The total required capacitance $C_{tot}$ of three DC-DC step-up/down converter topologies as a function of the output power $P_{out}$ . These values are obtained by means of SPICE-simulations, such that the three converters meet with the specifications of Table 3.13 . . . . .	99
Fig. 3.27	The model of an ideal transformer $Tr$ , together with its magnetizing inductance $L_M$ . . . . .	100
Fig. 3.28	(a) The circuit for calculating the energy transfer of $Tr$ and (b) the equivalent T-circuit, both in the Laplace-domain . . . . .	101
Fig. 3.29	(a) $i_{prim}(t)$ and $u_{out}(t)$ , (b) $E_{U_{in}}(t)$ and $E_{R_2}(t)$ and (c) $\eta_{Tr}(t)$ as a function of time $t$ , different values of coupling factor $k_M$ . . . . .	102
Fig. 3.30	The circuit of an ideal forward DC-DC converter . . . . .	102
Fig. 3.31	The circuit of an ideal full-bridge buck DC-DC converter . . . . .	103
Fig. 3.32	The circuit of an ideal push-pull boost DC-DC converter . . . . .	103
Fig. 3.33	The circuit of an ideal flyback DC-DC converter . . . . .	104
Fig. 3.34	The circuit of an ideal series resonant DC-DC converter . . . . .	105
Fig. 3.35	The voltage conversion ratio $k(f_{SW})$ as a function of the switching frequency $f_{SW}$ , for a series resonance DC-DC converter . . . . .	105
Fig. 3.36	(a) The circuit of a halve-bridge galvanic separated series resonance DC-AC high-voltage converter for the FAIMS setup. (b) $U_{out}$ of the DC-AC converter as a function of $t$ . (c) A photograph of the realization of the DC-AC converter . . . . .	106
Fig. 3.37	The concept of multi-phase DC-DC converters . . . . .	107
Fig. 3.38	The example of how a two-phase DC-DC converter can achieve a higher power conversion efficiency $\eta_{SW}$ than a single-phase DC-DC converter, at the same output power $P_{out}$ . . . . .	108
Fig. 3.39	(a) The timing signals of a two-phase converter and (b) the equivalent representation with sine waves, assuming that the converter is operating in CCM . . . . .	109
Fig. 3.40	The circuit of an ideal $n$ -phase boost DC-DC converter . . . . .	110
Fig. 3.41	(a) The current $i_C(t)$ through the output capacitor $C$ of a 2-phase boost converter for $\delta < 50\%$ and (b) for $\delta > 50\%$ , both valid for CCM. $i_C(t)$ is divided into the respective parts from the first ( <i>black curve</i> ) and second converter ( <i>gray curve</i> ) . . . . .	111
Fig. 3.42	The output voltage ripple $\Delta U_{out}$ as a function of the duty-cycle $\delta$ for an ideal 1-phase, 2-phase and 4-phase boost DC-DC converter. For the 1-phase and 2-phase boost converter both the exact and approximated functions are plotted. For the 2-phase and 4-phase boost converter the approximated functions are plotted . . . . .	112
Fig. 3.43	The circuit of an ideal $n$ -phase buck DC-DC converter . . . . .	113
Fig. 3.44	(a) The respective currents $i_{L1}(t)$ and $i_{L2}(t)$ through inductors $L_1$ and $L_2$ of a 2-phase buck converter for $\delta < 50\%$ and (b) for $\delta > 50\%$ , both valid for CCM . . . . .	114

Fig. 3.45 The output voltage ripple  $\Delta U_{out}$  as a function of the duty-cycle  $\delta$  for an ideal 1-phase, 2-phase and 4-phase buck DC-DC converter. For the 1-phase and 2-phase buck converter both the exact functions are plotted. For the 2-phase and 4-phase buck converter the approximated functions are plotted . . . . . 115

Fig. 3.46 The concept of Single-Inductor Multiple-Output (SIMO) DC-DC converters . . . . . 116

Fig. 3.47 The circuit of an ideal SIMO boost DC-DC converter with  $n$  outputs . . . . . 117

Fig. 3.48 The circuit of an ideal SIMO buck DC-DC converter with  $n$  outputs . . . . . 117

Fig. 3.49 The circuit of an ideal DC-DC boost Series Multiple Output Converter (SMOC) with  $n$  outputs . . . . . 118

Fig. 3.50 The circuit of an ideal DC-DC buck Series Multiple Output Converter (SMOC) with  $n$  outputs . . . . . 120

Fig. 4.1 The circuit of a boost DC-DC converter with all its resistive losses . . . . . 125

Fig. 4.2 **(a)** The equivalent circuit of the charge phase and **(b)** discharge phase of the inductor  $L$  for a boost DC-DC converter with all its resistive losses . . . . . 125

Fig. 4.3 The current  $i_{SW2}(t)$  through  $SW_2$  as a function of time  $t$  for a boost converter in steady-state DCM is shown by the *gray curve*, the *black curve* shows its linear approximation . . . . . 128

Fig. 4.4 The voltage  $u_C(t)$  over  $C$  as a function of time  $t$  for a boost converter in steady-state DCM is shown by the *gray curve*, the *black curve* shows its piecewise linear approximation . . . . . 128

Fig. 4.5 The circuit of a buck DC-DC converter with all its resistive losses . . . . . 131

Fig. 4.6 **(a)** The equivalent circuit of the charge phase and **(b)** discharge phase of the inductor  $L$  for a buck DC-DC converter with all its resistive losses . . . . . 132

Fig. 4.7 The current  $i_L(t)$  through  $L$  as a function of time  $t$  for a buck converter in steady-state DCM is shown by the *gray curve*, the *black curve* shows its linear approximation . . . . . 133

Fig. 4.8 The voltage  $u_C(t)$  over  $C$  as a function of time  $t$  for a buck converter in steady-state DCM is shown by the *gray curve*, the *black curve* shows its piecewise linear approximation . . . . . 134

Fig. 4.9 The lumped model for a metal-track or bondwire inductor, taking both the parasitic series resistance  $R_{L_s}$  and parasitic substrate capacitance  $C_{sub}$  into account . . . . . 136

Fig. 4.10 **(a)** The top-view of a planar square spiral inductor above a conductive substrate and **(b)** the cross-sectional view with indication of the most significant mutual inductances . . . . . 137

Fig. 4.11 The perpendicular cross-sectional view of a conductor which is prone to the skin-effect . . . . . 139

Fig. 4.12	The <i>black curve</i> shows the series resistance $R_{bondwire}$ per millimeter of length $\ell$ for a gold bondwire with $r = 12.5 \mu\text{m}$ , as a function of frequency $f$ and the <i>gray curve</i> denotes the DC value . . . . .	140
Fig. 4.13	The model for a capacitor, taking the parasitic series resistance $R_{Cs}$ , the parasitic parallel resistance $R_{Cp}$ and the parasitic series inductance $L_{Cs}$ into account . . . . .	142
Fig. 4.14	The output voltage $u_{out}(t)$ of a boost converter in <b>(a)</b> DCM and <b>(b)</b> CCM, as a function of time $t$ . The <i>gray curves</i> are valid for $R_{Cs} = 0$ and the <i>black curves</i> for a finite value of $R_{Cs}$ . . . . .	143
Fig. 4.15	The output voltage $u_{out}(t)$ of a buck converter in <b>(a)</b> DCM and <b>(b)</b> CCM, as a function of time $t$ . The <i>gray curves</i> are valid for $R_{Cs} = 0$ and the <i>black curves</i> for a finite value of $R_{Cs}$ . . . . .	144
Fig. 4.16	The parallel circuit of two capacitors $C_1$ and $C_2$ , with their respective parasitic series resistances $R_1$ and $R_2$ , and the equivalent circuit with one capacitor $C_{eq}(f)$ and resistor $R_{eq}(f)$ . . . . .	145
Fig. 4.17	The <i>upper graph</i> shows the equivalent capacitance $C_{eq}(f)$ and the <i>lower graph</i> shows the equivalent resistance $R_{eq}(f)$ , both as a function of frequency $f$ . . . . .	146
Fig. 4.18	The power loss $P_{Df}$ of forward voltage drop of a diode ( <i>black curve</i> ) and the power loss $P_{Ron}$ of the on-resistance of a MOSFET ( <i>gray curve</i> ), both as a function of the current $I$ . . . . .	147
Fig. 4.19	The parasitic capacitances in an n-MOSFET . . . . .	148
Fig. 4.20	The currents $i_{SW1}(t)$ and $i_{SW2}(t)$ through $SW_1$ and $SW_2$ and the voltages $u_{SW1}(t)$ and $u_{SW2}(t)$ over $SW_1$ and $SW_2$ for a boost converter in <b>(a)</b> DCM and <b>(b)</b> CCM . . . . .	150
Fig. 4.21	The currents $i_{SW1}(t)$ and $i_{SW2}(t)$ through $SW_1$ and $SW_2$ and the voltages $u_{SW1}(t)$ and $u_{SW2}(t)$ over $SW_1$ and $SW_2$ for a buck converter in <b>(a)</b> DCM and <b>(b)</b> CCM . . . . .	151
Fig. 4.22	The physical cross-sections <b>(a)</b> of the freewheeling p-MOSFET in a boost converter and <b>(b)</b> the freewheeling n-MOSFET in a buck converter. In both cross-sections the bulk current, which occurs at the transition between the charge and discharge phase, is shown . . . . .	153
Fig. 4.23	The circuit of a digital tapered CMOS buffer with $n$ -stages . . . . .	153
Fig. 4.24	A perspective view of a square metal-track conductor, with the definition of its width $W_{track}$ , its length $L_{track}$ and its thickness $d$ . . . . .	155
Fig. 4.25	<b>(a)</b> The model for the parasitic input resistance $R_{in}$ and inductance $L_{in}$ , with an on-chip decouple capacitor $C_{dec}$ and its parasitic series resistance $R_{Cdec}$ . <b>(b)</b> The equivalent impedance circuit of this model . . . . .	156
Fig. 4.26	The on-chip input voltage ripple $\Delta U_{in}$ as a function of the capacitance of the decouple capacitor $C_{dec}$ , for three different values of the parasitic series resistance $R_{Cdec}$ of the decouple capacitor. The parameters for which this plot is valid are given in Table 4.1 . . . . .	157

Fig. 4.27 The flow-chart of the model flow for the boost and the buck converter, starting from the differential equations and taking all the significant resistive and dynamic losses into account, except for the temperature effects . . . . . 162

Fig. 4.28 The flow-chart showing the additional flow to take the temperature and self-heating effects into account for the model of the boost and the buck converter . . . . . 163

Fig. 4.29 The qualitative design trade-offs for monolithic DC-DC converters: **(a)**  $f_{SW}$  as a function of  $L$  for different values of  $C$ , **(b)**  $\eta_{SW}$  as a function of  $L$  for different values of  $C$ , **(c)**  $I_{L\_max}$  and  $I_{L\_min}$  as a function of  $L$  for different values of  $C$ , **(d)**  $A_L$  as a function of  $L$ , for different values of  $R_{Ls}$ , **(e)**  $\eta_{SW}$  as a function of  $A_L$  for different values of  $C$ , **(f)**  $f_{SW}$  as a function of  $C$  for different values of  $R_{Cs}$ , **(g)**  $\Delta U_{out}$  as a function of  $C$  for different values of  $R_{Cs}$  and **(h)**  $\eta_{SW}$  as a function of  $C \sim A_C$ , for different values of  $R_{Cs}$  . . . . . 166

Fig. 5.1 The concept of a control system for an inductive DC-DC converter . . . . . 170

Fig. 5.2 The concept of Pulse Width Modulation (PWM) signal  $\Phi_1$  generation by means of comparing a triangular waveform  $U_{tria}$  to an error-voltage  $U_{err}$  . . . . . 171

Fig. 5.3 The basic principle of subharmonic oscillations in a DC-DC converter with a PWM control loop . . . . . 172

Fig. 5.4 The block diagram of the PWM control system implementation of a fully-integrated boost converter [Wen07] . . . . . 173

Fig. 5.5 The circuit of a symmetrical cascoded OTA with a current-loaded common emitter output stage . . . . . 174

Fig. 5.6 The circuit of a comparator . . . . . 174

Fig. 5.7 The circuit of a time-delay . . . . . 175

Fig. 5.8 The circuit of a level-shifter [Ser05] . . . . . 175

Fig. 5.9 The concept of Pulse Frequency Modulation (PFM), with a constant on-time  $t_{on}$ . The *upper graph* shows the timing for low load, low frequency operation and the *lower graph* shows the timing for high load, high frequency operation . . . . . 176

Fig. 5.10 The power conversion efficiencies  $\eta_{SW\_PFM}$  and  $\eta_{SW\_PWM}$  of a PFM (constant  $t_{on}$ ) and a PWM controlled DC-DC (*gray curve*) converter, as a function of the output power  $P_{out}$ . The *solid black curve* and the *dashed black curve* denote  $\eta_{SW\_PFM}$  for equal switching frequencies  $f_{SW\_PFM} = f_{SW\_PWM}$  at the maximal output power  $P_{out\_max}$  and at the minimal output power  $P_{out\_min}$ , respectively . . . . . 177